

# Notice of Allowability

Application No.

10/706,200

Examiner

Zia R. Hashmi

Applicant(s)

FABINSKI ET AL.

Art Unit

2881

## -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 8/16/2004.
2. ☒ The allowed claim(s) is/are 1-7.
3. ☒ The drawings filed on 12 November 2003 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All b) ☐ Some\* c) ☐ None of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

### Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

## **DETAILED ACTION**

### ***Allowable Subject Matter***

1. An "Amendment" was received on August 16, 2004 in response to Office Action of May 21, 2004. Independent claim 1 has been amended, as indicated.

2. Claims 1-7 are allowed.

3. The following is an examiner's statement of reasons for allowance:

With respect to amended independent claim 1, prior art fails to disclose a method for creating a pattern on a substrate, the method includes the steps of imprinting a first pattern on the substrate; and imprinting a second substantially similar pattern which is intentionally mis-registered in a pre-defined manner with regard to the first pattern so that the combination of the first and second patterns causes a systematic variation in a final size of defined elements across the substrate. Currently, the prior art addresses only the elimination of systematic variations in critical dimension feature size of lithographically defined images, which are sometimes, required to be compensated for process variability in the semiconductor industry. Such techniques, however, are subject to limitation of the mask writing tool address grid, or spot size, when determining the minimum possible difference within a pattern. The present invention overcomes this problem by creating a pattern on a substrate by the method described above. The present invention has the following advantages: varying the feature size in resist across the chip without the artifact of grid-snapping from the mask-writing tool; and the

incremental difference in feature dimension allowed by this method is so small as to be prohibitive (i.e. very small spot size) with the current mask-writing technology.

### ***Conclusion***

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments of Statement of Reasons for Allowance".
5. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact Electronic Business Center (EBC) at 866-217-9197 (toll-free).
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zia Hashmi whose telephone number is (571) 272-2473. The examiner can normally be reached between 8.30 AM- 5 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John R. Lee can be reached on (571) 272-2477.

Zia Hashmi

September 23, 2004

  
JOHN R. LEE  
SUPERVISOR, PATENT EXAMINER  
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